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TECHNOLOGY CENTER 2800IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.
Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
Docket No.: 1303.035US1
Filed: December 20, 2001
Examiner: Serial No.: 10/028,001
Due Date: N/A
Group Art Unit: 2818

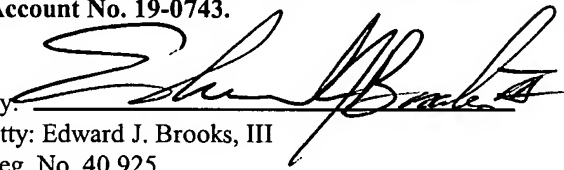
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Information Disclosure Statement (1 pg.), Form 1449 (3 pgs.), and copies of 41 cited references.
- ☒ A Communication Concerning Co-Pending Applications (2 pgs.).
- ☒ Copies of Co-Pending Applications (7 copies.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: 
Atty: Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 13 day of June, 2002.

Gina M. Uphus

Name

Signature

Customer Number 21186

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

(GENERAL)

S/N 10/028,001



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al. Examiner:
Serial No.: 10/028,001 Group Art Unit: 2818
Filed: December 20, 2001 Docket: 1303.035US1
Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL
DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date

6/11/2002

By

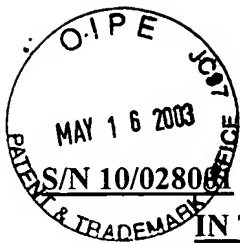
Edward J. Brooks, III
Reg. No. 40,925

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Gina M Unhus

Name

Signature



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al. Examiner: Tu-Tu Ho
Serial No.: 10/028,001 Group Art Unit: 2818
Filed: December 20, 2001 Docket: 1303.035US1
Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL
DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

#8 Suppl.
IDS
rhl
5/22/03

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. § 1.97(c)(2), please charge Deposit Account No. 19-0743 in the amount of \$180.00 for the fee set forth in 37 C.F.R. § 1.17(p).

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

05/19/2003 CCHAU1 00000042 190743 10028001
01 FC 1006 180.00 CH

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Date 5-14-03

By Mar L Beekman
Marvin L. Beekman
Reg. No. 38,377

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Name Amy Moriarty

Signature Amy Moriarty

S/N 10/028,001

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner:

Serial No.: 10/028,001

Group Art Unit: 2818

Filed: December 20, 2001

Docket: 1303.035US1

Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL
DEVICES AND ASYMMETRICAL TUNNEL BARRIERS



COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Commissioner for Patents
Washington, D.C. 20231

Noted, AH

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TECHNOLOGY CENTER 2800

Applicant would like to bring to the Examiner's attention the following related co-pending application(s) in the above-identified patent application:

<u>Serial No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/943,134	08/30/2001	01303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945,498	08/30/2001	01303.024US1	DEAPROM WITH INSULATING METAL OXIDE INTERPOLY INSULATORS
09/945,512	08/30/2001	01303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945,500	08/30/2001	01303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945,507	08/30/2001	01303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945,514	08/30/2001	01303.015US1	GRADED COMPOSITION GATE INSULATORS TO REDUCE TUNNELING BARRIERS IN FLASH MEMORY DEVICES

COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 10/028,001

Filing Date: December 20, 2001

Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

Page 2

Dkt: 1303.035US1

08/903,453 07/29/1997 00303.378US1

CARBURIZED SILICON GATE
INSULATORS FOR INTEGRATED
CIRCUITS

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

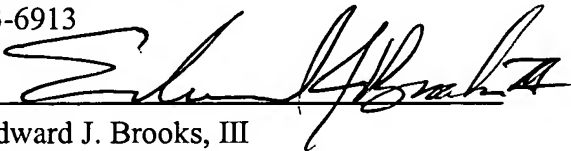
Minneapolis, MN 55402

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Name

Gina M. Uphus

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